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1 Personal computer (PC) thermal analyzer 100%
James M. Vaccaro , Douglas J. Holzhauer
Proceedings of the third international conference on Industrial and engineering applications of artificial intelligence and expert systems - Volume 2 June 1990

2 Synchronous path analysis in MOS circuit simulator 100%
Vishwani D. Agrawal
Proceedings of the nineteenth design automation conference January 1982
For verifying the timing performance of synchronous MOS circuits a path analysis facility has been developed in the MOTIS (MOS Timing Simulator) system. This path analysis traces the clock signals to the latches in the circuit, computes the clock skews and then performs a path search analysis between all latches. For the paths between clocked latches, the timing constraints are determined using the clock skews and the operating frequency. The paths that do not satisfy these constrain ...

3 Operational features of an MOS timing simulator 100%
P. Kozak , H. K. Gummel , B. R. Chawla
Proceedings of the 12th design automation conference January 1975
This paper describes operational features of a timing simulator having performance characteristics between those of circuit analysis programs and conventional logic simulators.

4 Man-machine interaction in the design of rotating electrical machines 100%

Bernard J. Bennington

Proceedings of the 6th annual conference on Design Automation January 1969

When engineering design is considered as a part of the more general study of system design or problem solving, it becomes apparent that it subdivides into the separate problems of design analysis, design synthesis and system identification. Rotating electrical machinery presents a uniquely complicated system of non-linear, constrained, discrete and discontinuous relationships. The economical solution of the design of electrical machines in our industrial society can only be achie ...

5 A real-time, multi-task programming language for microprocessor-based industrial process control 100%

Alfred C. Weaver

Proceedings of the 1978 annual conference - Volume 2 January 1978

This paper presents an overview of the design of a real-time programming language whose purpose is to permit an inexperienced programmer to quickly and efficiently implement control of multiple, parallel industrial processes. The programming language is compiled on one microprocessor-based system and then executed on another. The language divides the program logic into two types: (1) combinational logic which requires both fast and frequent execution, and (2) sequential logic which is more ...

6 A real-time/time-share computer in a research and development environment 100%

C. D. Longerot , J. E. Marceau

Proceedings of the 1971 26th annual conference January 1971

A centralized computer with high speed peripherals, mass storage and very flexible input/output ports provides eighteen remote laboratory terminals with real-time/time-share computer service. The EMR 6130 Computer with Sandia designed interfacing provides real-time response in research and development activities involving on-line data acquisition, analysis and display, and includes features which allow process control and equipment programming activities. The system supports a variety of co ...

7 Use of simulation in support of development and testing of submarine subsystems 100%

James O. Goodburn , Robert A. Massarotti

Proceedings of the eleventh annual simulation symposium March 1978

The purpose of this paper is to describe an existing real-time digital simulation which is utilized in the testing and integration of submarine subsystems. The testing and integration effort involves both the hardware and software verification. Advanced fire control systems are not only composed of new hardware but also larger and more sophisticated software systems. The only way to test and check-out these systems in a laboratory environment is with simulation. The simulation provides dyna ...

8 Fable: A programming-language solution to IC process automation problems 100%

Harold L. Ossher , Brian K. Reid

Proceedings of the 1983 ACM SIGPLAN symposium on Programming language issues in software systems June 1983

The Stanford University Center for Integrated Systems is embarking on an

ambitious project to formally characterize integrated circuit fabrication processes, and to provide a degree of automation of research and prototyping activities in the IC fabrication facility. A crucial component of this project is the ability to represent an IC fabrication "recipe" in a repeatable, transportable, device-independent fashion. We have designed the language Fable for this purpose: it offers s ...

9 Three ECL designs for microprogrammable Writable Control Stores 100%

J. F. McDonald , R. Harris , J. Sustman

Conference record of the sixth annual workshop on Microprogramming September 1973

Three designs are presented for extremely fast microprogrammed timing and control sequencers driven by Writable Control Stores. These designs have been put forth with a view towards utilizing existing or impending developments in the field of Emitter Coupled Logic (ECL). One of the designs is directly applicable to an existing ECL minicomputer architecture (that of the Digital Scientific META-4). The other two are more conjectural. One of these modules has a parts cost of roughly only &doll ...

10 Design considerations for a computer-based clinical physiologic research system 100%

Ronald W. Hagen , Lewis J. Thomas , Janet A. Johnson

Proceedings of the annual conference October 1976

Experience in the design of computer-based patient monitoring and clinical physiologic research systems is drawn upon to suggest some useful design strategies and architectural configurations for such systems. Emphasis is placed on flexibility as an over-riding consideration for research systems in contrast to the level of specialization appropriate to monitoring systems. The previously undescribed clinical-research system is detailed as necessary to show where differences in both hardware ...

11 Simulation hierarchy for microprocessor design 100%

Will Sherwood

Proceedings of the Symposium on Design Automation and Microprocessors February 1977

There are many levels of abstraction through which a designer passes when implementing a microprocessor chip set or system. He usually begins by configuring the application for the microprocessor, bus, and peripherals (memory, etc.). Section at a time, he expands the system components into a Register Transfer level diagram, followed by a detailed chip or gate description. This paper will show how a hierarchical simulator aids each phase in the design by modeling elements at all levels from ...

12 Dames an integrated systems approach to computer-aided design of electronic systems 100%

Robert Lewis , Ronald Segal

Proceedings of the fifth annual 1968 design automation workshop on Design automation July 1968

Parallel with the increasing acceptance and utilization of microelectronic techniques has come a corresponding increase in the complexity of required circuits and in the number of factors to be considered when formulating and implementing a design. When one considers that many steps in the design process are repetitive, and that data gathering and documentation occupy the largest percent of the engineering time-cycle, it becomes clear that more help can and must be provided for the designer ...

13 A mixed-mode simulator 100%

V. D. Agrawal , A. K. Bose , P. Kozak , H. N. Nham , E. Pacas-Skewes

Proceedings of the seventeenth design automation conference on Design automation June 1980

To provide flexibility and efficiency in logic and timing verification of MOS VLSI circuits, it is desirable that various portions of a circuit can be described and simulated at appropriate levels of detail. Such a capability is provided by the Mixed-Mode Simulator described here. This simulator allows different elements of a circuit to be modeled and simulated at different levels of detail. The modeling levels are MOS transistor level, logic gate level and functional level. The simul ...

14 A microprocessor based tea dryer controller 100%

S. S.S.P. Rao , V. K. Agarwal

Proceedings of the 3rd ACM SIGSMALL symposium and the first SIGPC symposium on Small systems September 1980

This paper reports in detail the design of a microprocessor based system for providing efficient and sophisticated control in tea processing operations. At first it discusses in brief the control strategies being followed by the Indian tea industry. All the monitoring and control activities of the tea processing are at present being done manually yielding typical throughputs of 80 kg/hr to 250 kg/hr. A proposal to optimise the process through automation by a microprocessor based system is p ...

15 Applications of digital processors to energy monitoring and control systems 100%

Alan A. Ross , John M. Borky

Proceedings of the 3rd ACM SIGSMALL symposium and the first SIGPC symposium on Small systems September 1980

The crisis in cost and availability of energy has led to the development of digital monitoring and control systems which manage and reduce energy consumption in a wide range of facilities. Large energy management systems incorporate distributed processing architectures and a wide range of manual and automatic functions. Design and implementation of such systems poses serious problems of function and algorithm definition, data communications, and optimization of physically dispersed processo ...

16 An automated procedure for developing hybrid computer simulations of turbofan engines 100%

John R. Szuch , Susan M. Krosel , William M. Bruton

Proceedings of the 14th annual simulation symposium March 1981

This paper offers a systematic, computer-aided, self-documenting methodology for developing hybrid computer simulations of turbofan engines. The methodology that is presented makes use of a host program that can run on a large digital computer and a machine-dependent target (hybrid) program. The host program performs all of the calculations and data manipulations that are needed to transform user-supplied engine design information to a form suitable for the hybrid computer. The host program ...

17 The theory of signature testing for VLSI 100%

J. Lawrence Carter

Proceedings of the fourteenth annual ACM symposium on Theory of computing May 1982

Several methods for testing VLSI chips can be classified as signature methods. Both conventional and signature testing methods apply a number of test patterns to the inputs of the circuit. The difference is that a conventional method examines each output, while a signature method first accumulates the outputs in some data compression device, then examines the signature - the final contents of the accumulator - to see if it agrees with the signature produced by a good chip. ...

18 An effective graphics user interface for rules and inference mechanisms 100%

J. W. Lewis

Proceedings of the SIGCHI conference on Human Factors in Computing Systems December 1983

As the technology of rule-based inference mechanisms matures, knowledge acquisition—the creation, structuring, and verification of rules—becomes increasingly important. The accuracy and completeness of the rules in the knowledge base determine expert system performance, and the cost of acquiring that knowledge base dominates all other hardware and software costs in practical systems. To reduce knowledge acquisition time and error rate, a new interactive graphics inter ...

19 An interactive graphics environment for architectural energy simulation 100%

Jon H. Pittman , Donald P. Greenberg

Proceedings of the 9th annual conference on Computer graphics and interactive techniques July 1982

An interactive computer graphics system has been developed for the architecture profession which provides a "design environment" for the evaluation of building energy consumption. The system includes an integrated set of graphic input tools which generate the geometric and attribute data necessary for the determination of thermal load in buildings. In addition, a comprehensive set of graphical output routines has been created to allow the designer to visually interpret the resul ...

20 Application of integration algorithms in a parallel processing environment for the simulation of jet engines 100%

Susan M. Krosel , Edward J. Milner

Proceedings of the fifteenth annual simulation symposium March 1982

The development of digital dynamic simulations requires careful selection of an appropriate integration algorithm. This paper illustrates the application of predictor-corrector integration algorithms developed for the digital parallel processing environment. The algorithms are implemented and evaluated through the use of a software simulator which provides an approximate representation of the parallel processing hardware. Test cases which focus on the use of the algorithms are presented and ...

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Nancy G. Leveson

ACM Computing Surveys (CSUR) June 1986

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High-performance computer technology is undergoing a period of unusually rapid change, and this paper attempts to describe the patterns of these changes in a systematic way. Pattern recognition is the basis of technology forecasting, and it is through technology forecasting that we obtain the anticipatory information that allows us to avoid problems and create opportunities. We will first identify the stages in which technological changes occur, and then define "change" as the f ...

38 Tablet: personal computer of the year 2000 100%

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41 Load balancing loosely synchronous problems with a neural network 100%
G. C. Fox , W. Furmanski
Proceedings of the third conference on Hypercube concurrent computers and applications: Architecture, software, computer systems, and general issues - Volume 1 January 1988
Hopfield and Tank have introduced the use of neural networks for the solution of optimization problems such as the traveling salesman problem. Here we show how to generalize this method to decompose loosely synchronous problems onto parallel machines and in particular the hypercube. In this case, decomposition or load balancing can be formulated graph theoretically in terms of optimal partitioning of the computational graph into N = 2

42 Task allocation onto a hypercube by recursive mincut bipartitioning 100%
F. Ercal , J. Ramanujam , P. Sadayappan
Proceedings of the third conference on Hypercube concurrent computers and applications: Architecture, software, computer systems, and general issues - Volume 1 January 1988
An efficient recursive task allocation scheme, based on the Kernighan-Lin mincut bisection heuristic, is proposed for the effective mapping of tasks of a parallel program onto a hypercube parallel computer. It is evaluated by comparison with an adaptive, scaled simulated annealing method. The recursive allocation scheme is shown to be effective on a number of large test task graphs - its solution quality is nearly as good as that produced by simulated annealing, and its computation time is ...

43 Communication-sensitive heuristics and algorithms for mapping compilers 100%

Bernd Stramm , Francine Berman
ACM SIGPLAN Notices , Proceedings of the ACM/SIGPLAN conference on Parallel programming: experience with applications, languages and systems
January 1988
Volume 23 Issue 9

The mapping problem arises when parallel algorithms are implemented on parallel machines. When the number of processes exceeds the number of available processing elements, the mapping problem includes the contraction problem. In this paper, we identify communication-sensitive heuristics which promote good contractions for graph-based parallel algorithms on non-shared memory multiprocessors. We present algorithms which utilize these heuristics and discuss their performance on a group of dive ...

44 Buffer management based on return on consumption in a multi-query environment 100%

Philip S. Yu , Douglas W. Cornell
The VLDB Journal — The International Journal on Very Large Data Bases
January 1993
Volume 2 Issue 1

In a multi-query environment, the marginal utilities of allocating additional buffer to the various queries can be vastly different. The conventional approach examines each query in isolation to determine the optimal access plan and the corresponding locality set. This can lead to performance that is far from optimal. As each query can have different access plans with dissimilar locality sets and sensitivities to memory requirement, we employ the concepts of memory consumption and return on cons ...

45 A new approach to the maximum-flow problem 100%

Andrew V. Goldberg , Robert E. Tarjan
Journal of the ACM (JACM) October 1988
Volume 35 Issue 4

All previously known efficient maximum-flow algorithms work by finding augmenting paths, either one path at a time (as in the original Ford and Fulkerson algorithm) or all shortest-length augmenting paths at once (using the layered network approach of Dinic). An alternative method based on the preflow concept of Karzanov is introduced. A preflow is like a flow, except that the total amount flowing into a vertex is allowed to exceed the total amount flowing out. The method m ...

46 Opportunities for research on numerical control machining 100%

David D. Grossman
Communications of the ACM May 1986
Volume 29 Issue 6

Numerical control (NC) machining could be reinvigorated by adapting robotic software technology. Regrettably, pressures are mounting in industry to constrain robots to NC standards, and the academic community views NC as an obsolete, solved problem, with little remaining scholarly challenge. Grossman examines the current status of APT, an NC language, and proposes the merging of APT with a modern robotics language.

47 Hierarchical representation and machine learning from faulty jet engine behavioral examples to detect real time abnormal conditions 100%

U. K. Gupta , M. Ali

Proceedings of the first international conference on Industrial and engineering applications of artificial intelligence and expert systems - Volume 2 June 1988

48 Using silicon and gallium arsenide technologies for new supercomputer design 100%

S. Nelson

Proceedings of the 2nd international conference on Supercomputing June 1988

A comparison is made between emerging high performance silicon and gallium arsenide technologies for the design and manufacture of the next supercomputers. Material, device, circuit, packaging, and manufacturing issues make comparisons complex and competing design methodologies will continue.

49 Folding RNA on the Cray-2 100%

Michael Ess

Proceedings of the 1990 ACM/IEEE conference on Supercomputing November 1990

Predicting RNA folding is a very computationally intensive task, that depends heavily on the assumptions of the model of folding. The 'stem list method' provides a flexible framework to change the assumptions of the model, but the price for this flexibility is its large computational costs. A C implementation of the 'stem list method' is given for the Cray-2 that takes advantage of both vectorization and multi-tasking. This implementation of exhaustive, depth first searching may have uses in oth ...

50 Survey of software tools for evaluating reliability, availability, and serviceability 100%

Allen M. Johnson , Miroslaw Malek

ACM Computing Surveys (CSUR) September 1988

Volume 20 Issue 4

In computer design, it is essential to know the effectiveness of different design options in improving performance and dependability. Various software tools have been created to evaluate these parameters, applying both analytic and simulation techniques, and this paper reviews those related primarily to reliability, availability, and serviceability. The purpose, type of models used, type of systems modeled, inputs, and outputs are given for each package. Examples of some of the key modeling ...

51 Modeling california earthquakes and earth structures 100%

Michael R. Raugh

Communications of the ACM November 1985

Volume 28 Issue 11

Seismology has burgeoned into a modern science—force-fed by federal funding to advance technology for detecting underground nuclear explosions and predicting earthquakes, and by industry to improve tools for gas and oil exploration. Computers, seismic instrument systems, telemetry, and data reduction have played key roles in this growth.

52 The art and science of visualizing data 100%

Karen A. Frenkel

Communications of the ACM February 1988

Volume 31 Issue 2

"I manipulate the laser," the artist said, having exploited laboratory equipment. "This is a parallel pipeline systolic SIMD engine we call the 'Jell-O Engine,'" the animator/straight man announced, but not until he had decimated the practice of ray tracing. And officials from supercomputer centers declared the visualization of scientific data would define a new field, a revolutionary way of doing science.

53 Strategic computing at DARPA: overview and assessment 100%

Mark Stefik

Communications of the ACM July 1985

Volume 28 Issue 7

Strategic Computing, a 10-year initiative to build faster and more intelligent systems, is ambitious, flawed by overscheduling perhaps and problems of definition, but basically sound.

54 Performance of a parallel algorithm for standard cell placement on the Intel hypercube 100%

M. Jones , P. Banerjee

24th ACM/IEEE conference proceedings on Design automation conference

October 1987

In this paper, we present a parallel simulated annealing algorithm for standard cell placement that is targeted to run on the Intel Hypercube. We present a novel tree broadcasting strategy that is used extensively in our algorithm for updating cell locations in the parallel environment. Studies on the performance of our algorithm on example industrial circuits show that it is faster and gives better final placement results than the uniprocessor simulated annealing algorithms.

55 Standard cell placement using simulated sintering 100%

L. K. Grover

24th ACM/IEEE conference proceedings on Design automation conference

October 1987

Simulated annealing is a powerful optimization technique based on the annealing phenomenon in crystallization. In this paper we propose a simulated sintering technique which is analogous to the sintering process in material processing. In sintering one improves the quality of a processed material by heating it to a temperature close to the melting point. Analogously, we show that by starting out with a good initial configuration instead of a random configur ...

56 PDOC - a database on paralel processing literature 100%

J.-Fr. Hake

ACM SIGARCH Computer Architecture News September 1985

Volume 13 Issue 4

A systematic and economic development of the large-scale computing environment at research centers has to be accompanied by some services providing a survey on the relevant literature. This paper deals with the imbedding of a database on 'High Speed Computing and Parallel Processing' literature into the computing environment at KFA Jülich.

57 IFIP Congress-62, Munich, Germany, August 27-September 1, 1962: Abstracts of papers 100%

Communications of the ACM June 1962

Volume 5 Issue 6

58 The CRAY-1 computer system 100%

Richard M. Russell
Communications of the ACM January 1978
Volume 21 Issue 1

This paper describes the CRAY-1, discusses the evolution of its architecture, and gives an account of some of the problems that were overcome during its manufacture. The CRAY-1 is the only computer to have been built to date that satisfies ERDA's Class VI requirement (a computer capable of processing from 20 to 60 million floating point operations per second) [1]. The CRAY-1's Fortran compiler (CFT) is designed to give the scientific user immediate access to the benefi ...

59 Laser optical disk: the coming revolution in on-line storage 100%

Larry Fujitani
Communications of the ACM June 1984
Volume 27 Issue 6

Commercially available only recently, the optical disk drive uses a laser beam to burn impressions onto a plastic disk. Employing a highly focused beam rather than a diffuse magnetic field to write, the laser optical disk drive yields storage densities up to 10 times those of magnetic disks.

60 From Electron Mobility to Logical Structure: A View of Integrated Circuits 100%

Wesley A. Clark
ACM Computing Surveys (CSUR) September 1980
Volume 12 Issue 3

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61 Implementation of a Convective Problem Requiring Auxiliary Storage 100%
J. H. Ericksen , R. Wilhelmson
ACM Transactions on Mathematical Software (TOMS) June 1976
Volume 2 Issue 2

62 Configuration control in an Ada programming support environment 100%
Mark Marcus , Kirk Sattley , C. Mugur Stefanescu
Proceedings of the Joint Ada conference fifth national conference on Ada technology and fourth Washington Ada Symposium March 1987

63 Computational astrophysics 100%
W. D. Arnett
Communications of the ACM April 1985
Volume 28 Issue 4
As computers become more powerful and sophisticated, computational astrophysicists will be able to find out more about stellar evolution and other astronomical phenomena.

64 Computers Then and Now 100%
Maurice V. Wilkes
Journal of the ACM (JACM) January 1968
Volume 15 Issue 1
Reminiscences on the early developments leading to large scale electronic computers show that it took much longer than was expected for the first of the more ambitious and fully engineered computers to be completed and prove

themselves in practical operation. Comments on the present computer field assess the needs for future development.

65 Rectangular spatial decomposition methods for parallel simulated annealing 100%

Dan R. Greening , Frederica Darema

Proceedings of the 3rd international conference on Supercomputing June 1986

Research on VLSI placement has extended the standard sequential simulated annealing technique to two multiprocessing variants. In one technique, processors perform moves on disjoint partitions of locally-stored circuit grids. In the other, processors perform simultaneous moves on a shared grid. Our research explores new techniques in the first category—called spatial decomposition algorithms. We describe the impact of cell mobility and cost-function errors in parallel simul ...

66 Developing instructional microcomputer laboratories for a university 100%

David J. Solomon , Susan M. Hazard

Proceedings of the 13th annual ACM SIGUCCSconference on User services: pulling it all together September 1985

Five microcomputer laboratories have been installed for general instructional use at Michigan State University. Each laboratory contains 16 fixed disc IBM™ PC-compatible microcomputers networked with the University's mainframe computer. In order to reduce costs and extend the hours the laboratories are available for student use, they are designed to be left unattended by Computer Laboratory staff. To accomplish this the laboratories have been made secure by storing the microcomputer s ...

67 Automatic placement a review of current techniques (tutorial session) 100%

Bryan T. Preas , Patrick G. Karger

Proceedings of the 23rd ACM/IEEE conference on Design automation July 1986

This review provides an overview of the placement function within automatic layout systems. The automatic placement problem is defined and the data abstractions are described. The discussion divides placement algorithms into two classes: constructive and iterative. Applications of the algorithms within layout systems are described. A large number of references is provided to allow use as a guide to placement literature.

68 Multiprocessor-based placement by simulated annealing 100%

Saul A. Kravitz , Rob A. Rutenbar

Proceedings of the 23rd ACM/IEEE conference on Design automation July 1986

Simulated annealing methods have proven to be particularly successful in physical design applications, but often require burdensome, long run times. This paper studies the design and analysis of standard cell placement by annealing in a multiprocessor environment. Annealing is not static: we observe that the temperature parameter which controls hill-climbing in simulated annealing changes the behavior of an annealing algorithm as it runs, and strongly influences the choice of multiprocessor ...

69 MIDAS: integrated CAD for total system design 100%

W. M. Budney , S. K. Holewa

Proceedings of the 22nd ACM/IEEE conference on Design automation June 1985

Control Data's Modular Integrated Design Automation System (MIDAS) is a highly integrated CAD system supporting the full range of activities required for the

design of complex digital systems. From schematic capture through design verification and manufacturing, MIDAS emphasizes a structured top down approach, from chips to supercomputers. MIDAS is fully hierarchical and is capable of managing and controlling the design of some of the world's largest computers, as well as speeding up the de ...

70 Hardware acceleration of gate array layout 100%

Philip M. Spira , Carl Hage

Proceedings of the 22nd ACM/IEEE conference on Design automation June 1985

In this paper we describe the hardware and software of a system which we have implemented to accelerate the physical design of gate arrays. In contrast to nearly all other reported approaches, our approach to hardware acceleration is to augment a single-user host workstation with a general-purpose microprogrammable slave processor having a large private memory. One or more such slaves can be attached. We have implemented placement improvement on the system, achieving a 20 x speedup vs. a hi ...

71 Clustering based simulated annealing for standard cell placement 100%

Sivanarayana Mallela , Lov K. Grover

Proceedings of the 25th ACM/IEEE conference on Design automation June 1988

Simulated annealing has been shown to be effective in producing good quality results for the standard cell placement problem. Its main drawback is the excessive computation time required, which increases significantly with the problem size. In this paper we present a novel technique for reducing the effective problem size for simulated annealing without compromising the solution quality. We form clusters of cells based on their interconnections, and place t ...

72 A defect-tolerant and fully testable PLA 100%

N. Wehn , M. Glesner , K. Caesar , P. Mann , A. roth

Proceedings of the 25th ACM/IEEE conference on Design automation June 1988

This paper presents a defect-tolerant and fully testable PLA allowing for the repair of a defective chip. The repair process is described. Special emphasis is devoted to the location of defects inside a PLA. The defect location mechanism is completely topological and circuit independent and therefore easy to adapt to existing PLA generators. Yield considerations for this type of PLAs are presented.

73 Solving minimum-cost flow problems by successive approximation 100%

A. Goldberg , R. Tarjan

Proceedings of the nineteenth annual ACM conference on Theory of computing January 1987

We introduce a framework for solving minimum-cost flow problems. Our approach measures the quality of a solution by the amount that the complementary slackness conditions are violated. We show how to extend techniques developed for the maximum flow problem to improve the quality of a solution. This framework allows us to achieve &Ogr;(min(n3, n5/3 m2/3, ...

74 Improving a multistage/multiprocessor flow-shop problem of numerous technological constraints through scheduling 100%

Way Kuo , Jon Yanney , Russell Tsai

Proceedings of the 17th conference on Winter simulation December 1985

The manufacturing of industrial rubber compounds is a three-stage process on a Banbury production system. At each stage the rubber is mixed (in a Banbury

mixer) and transferred to next-stage storage. Depending on requirements, the first two stages may be repeated up to three times. Finally, rubber is mixed on the third stage and then milled to obtain a slab form of the new compound rubber. The objective is to derive a "good" heuristic scheduling algorithm that uses a ...

75 Uniting probabilistic methods for optimization 100%

Bennett L. Fox
Proceedings of the 24th conference on Winter simulation December 1992

76 APL helps the deaf to hear again 100%

Pierre Deslauriers
ACM SIGAPL APL Quote Quad , Proceedings of the international conference on APL September 1993
Volume 24 Issue 1

This paper describes the role of APL as an efficient and crucial tool in research and development of sophisticated electronic systems. It will show how APL was successfully used in the development of a cochlear implant device. Cochlear implants are bio-medical electronic systems allowing completely deaf persons to recover partial hearing capabilities. This kind of system has been around for some time. Unfortunately, performance and flexibility have improved at a slow pace. Also, a more in-depth ...

77 Full-screen, scrollable APL2 spreadsheet input/output editor 100%

Peter A. W. Lewis
ACM SIGAPL APL Quote Quad March 1993
Volume 23 Issue 3

A full-screen, scrollable, spreadsheet-like editor based on IBM's APL2 32-bit interpreter for 386/486-based microcomputers is described. It is used for entering, examining, analyzing, editing and printing data. Mixed numeric and character arrays can be read in from or written out to formatted DOS files (ASCII) or comma-delimited DOS files. Alternatively, a bulk mode input facility allows for rapid direct data entry, or data can be entered, examined and edited cell-by-cell in the usual way. A fac ...

78 Random current testing for CMOS logic circuits by monitoring a dynamic power supply current 100%

Hideo Tamamoto , Hiroshi Yokoyama , Yuichi Narita
Proceedings of the conference on European Design Automation November 1992

79 Some computer science issues in ubiquitous computing 100%

Mark Weiser
Communications of the ACM July 1993
Volume 36 Issue 7

80 A Markovian framework for digital halftoning 100%

Robert Geist , Robert Reynolds , Darrell Suggs
ACM Transactions on Graphics (TOG) April 1993
Volume 12 Issue 2

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81 The Alpha demonstration unit: a high-performance multiprocessor 100%
Charles P. Thacker , David G. Conroy , Lawrence C. Stewart
Communications of the ACM February 1993
Volume 36 Issue 2

82 Multitasking simulation of a boiler system using qualitative model-based reasoning 100%
Yuh-Jeng Lee , James F. Stascavage
ACM Transactions on Modeling and Computer Simulation (TOMACS) October 1992
Volume 2 Issue 4

83 Mapping applications onto a cache coherent multiprocessor 100%
A. K. Nanda , L. N. Bhuyan
Proceedings of the 1992 ACM/IEEE conference on Supercomputing December 1992

84 Performance of a plasma fluid code on the Intel parallel computers 100%
V. E. Lynch , B. A. Carreras , J. B. Drake , J. N. Leboeuf , P. Liewer
Proceedings of the 1992 ACM/IEEE conference on Supercomputing December 1992

85 Sci-fi at CHI: Cyberpunk novelists predict future user interfaces 100%
Aaron Marcus , Donald A. Norman , Rudy Rucker , Bruce Sterling , Vernor Vinge
Proceedings of the SIGCHI conference on Human factors in computing systems June 1992
This plenary panel will explore ideas about future user interfaces, their technology support, and their social context as proposed in the work of leading authors of science fiction characterized as the Cyberpunk movement. Respondents will react to and comment upon the authors' presentations.

86 A logic base tool set for real-time Ada software development 100%
Michael Moore
Proceedings of the eighth annual Washington Ada symposium & summer SIGAda meeting on Ada: software: foundation for competitveness June 1991
This is a report on work conducted privately that explores the use of predicate logic to reason about real-time design. Safety and reliability issues associated with embedded real-time systems make greater demands on development engineers than non-real-time systems whose functional complexity is of similar degree. The effort undertaken here attempts to provide methods and tools for dealing with both the functional and temporal aspects of software engineering. The goal is to improve the effe ...

87 SPLASH: Stanford parallel applications for shared-memory 100%
Jaswinder Pal Singh , Wolf-Dietrich Weber , Anoop Gupta
ACM SIGARCH Computer Architecture News March 1992
Volume 20 Issue 1
We present the Stanford Parallel Applications for Shared-Memory (SPLASH), a set of parallel applications for use in the design and evaluation of shared-memory multiprocessing systems. Our goal is to provide a suite of realistic applications that will serve as a well-documented and consistent basis for evaluation studies. We describe the applications currently in the suite in detail, discuss some of their important characteristics, and explore their behavior by running them on a real multiprocess ...

88 Solving combinatorial optimization problems using parallel simulated annealing and parallel genetic algorithms 100%
Pooja P. Mutalik , Leslie R. Knight , Joe L. Blanton , Roger L. Wainwright
Proceedings of the 1992 ACM/SIGAPP symposium on Applied computing: technological challenges of the 1990's March 1992

89 SIDECAR: design support for reliability 100%
Charles R. Yount , Daniel P. Siewiorek
Proceedings of the 28th conference on ACM/IEEE design automation conference June 1991

90 Time multiplexed optical computers 100%
Harry F. Jordan , Vincent P. Heuring
Proceedings of the 1991 ACM/IEEE conference on Supercomputing August 1991

91 High performance vector processing in reservoir simulation 100%
L. C. Young , S. E. Zarantonello
Proceedings of the 1991 ACM/IEEE conference on Supercomputing August

1991

92 Nuclear power plant diagnostics in APL 100%

Alexander O. Skomorokhov

ACM SIGAPL APL Quote Quad , Proceedings of the international conference on APL '91 July 1991

Volume 21 Issue 4

We are interested in the development of Nuclear Power Plant (NPP) diagnostic systems and other complex systems of data processing. There are some questions on the subject:How to build these systems easily?How to build them fast?How to build them at a low price?And how to build them to be user friendly?Today, from our point of view, in the area of Nuclear Power Plant diagnostics, there is only one answer to these questions: We must use APL.

93 Domain composition methods for associating geometric modeling with finite element modeling 100%

J. J. Cox , W. W. Charlesworth , D. C. Anderson

Proceedings of the first ACM symposium on Solid modeling foundations and CAD/CAM applications May 1991

94 Real-time disturbance control 100%

B. Chandrasekaran , R. Bhatnager , D. D. Sharma

Communications of the ACM August 1991

Volume 34 Issue 8

95 The impact of operating system scheduling policies and synchronization methods of performance of parallel applications 100%

Anoop Gupta , Andrew Tucker , Shigeru Urushibara

ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1991 ACM SIGMETRICS conference on Measurement and modeling of computer systems April 1991

Volume 19 Issue 1

96 VLSI cell placement techniques 100%

K. Shahookar , P. Mazumder

ACM Computing Surveys (CSUR) June 1991

Volume 23 Issue 2

VLSI cell placement problem is known to be NP complete. A wide repertoire of heuristic algorithms exists in the literature for efficiently arranging the logic cells on a VLSI chip. The objective of this paper is to present a comprehensive survey of the various cell placement techniques, with emphasis on standard cell and macro placement. Five major algorithms for placement are discussed: simulated annealing, force-directed placement, min-cut placement, placement by numerical optimization, a ...

97 Two-dimensional compaction by "zone refining" 88%

Hyunchul Shin , Alberto L. Sangiovanni-Vincentelli , Carlo H. Séquin

Proceedings of the 23rd ACM/IEEE conference on Design automation July 1986

A new technique for 2-dimensional layout compaction of integrated circuits is presented. After a traditional one-dimentional precompaction step, the size of the layout is further reduced with a technique that bears a strong similarity to

the technique of 'zone-refining' used in the purification of crystal ingots. Individual circuit components or small clusters of components are peeled off row by row from the precompacted layout, moved across an open zone, and reassembled at the other end of ...

98 Chip-planning, placement, and global routing of macro/custom cell integrated circuits using simulated annealing 84%

Carl Sechen

Proceedings of the 25th ACM/IEEE conference on Design automation June 1988

The algorithms and the implementation of a new macro/custom cell chip-planning, placement, and global routing package are presented. The simulated-annealing-based placement algorithm proceeds in two stages. In the first stage, the interconnect area around the individual cells is determined using a new dynamic interconnect area estimator. The second stage consists of: (1) a channel definition step, using a new channel definition algorithm, (2) a global routing step, using a new global router ...

99 Integrated placement for mixed macro cell and standard cell designs 84%

Michael Upton , Khosrow Samii , Stephen Sugiyama

Conference proceedings on 27th ACM/IEEE design automation conference January 1991

This paper presents an approach to the automatic placement of a combination of macro blocks and standard cells. Standard cells are partitioned into flexible virtual blocks during block placement and are later placed into the target area through an integrated optimization routine. Results for a number of examples are given, including those from standard placement benchmarks.

100 Computer designed multilayer hybrid substrate using thick film technology 80%

Chester W. Waldvogel

Proceedings of the 14th design automation conference January 1977

State of the art system designs require larger, more densely populated, thermally stable, multilayer hybrid substrates. Increased logic densities dictate the need for narrower conductor line widths and better screening techniques. Increasing material and labor costs, as well as component shortages, are also major considerations in the efficient design of complex substrates. Presented herein are the materials, screening techniques, and process steps required to fabricate a densely populated ...

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101 Time constrained planning using simulated annealing 77%
D. J. Goehring
Proceedings of the first international conference on Industrial and engineering applications of artificial intelligence and expert systems - Volume 2 June 1988

102 Simulation: the small manufacturer's unknown need 77%
Walter J. Trybula
Proceedings of the 22nd conference on Winter simulation December 1990

103 GENIE: a generalized array optimizer for VLSI synthesis 77%
Srinivas Devadas , A. R. Newton
Proceedings of the 23rd ACM/IEEE conference on Design automation July 1986
A new generalized array optimization scheme is presented which solves the problem of efficient automatic layout of multi-level CMOS and NMOS logic circuits. The new approach has been implemented in the program GENIE which can be used for the multiple folding of PLAS, as well as for compacting gate matrix layouts, SLAs, and Weinberger arrays. The cells in the array can be of non-uniform sizes and any form of constraint can be placed on the input and output terminals. The generalized array op ...

104 TimberWolf3.2: a new standard cell placement and global routing package 77%
Carl Sechen , Alberto Sangiovanni-Vincentelli
Proceedings of the 23rd ACM/IEEE conference on Design automation July 1986

TimberWolf3.2 is a new standard cell placement and global routing package. The placement and global routing proceed over 3 distinct stages. The general combinatorial optimization technique known as simulated annealing is used during the first two stages of the placement. In the first stage, TimberWolf3.2 places the cells such that the total estimated interconnect cost is minimized. During the second stage, TimberWolf3.2 inserts feed through cells as required and the minimization of the tota ...

105 Automatic differentiation in circuit simulation and device modeling 77%

Peter Feldmann , Robert Melville , Shahriar Moinian
Proceedings of the 1992 IEEE/ACM international conference on Computer-aided design November 1992

106 Performance of a new annealing schedule 77%

Jimmy Lam , Jean-Marc Delosme
Proceedings of the 25th ACM/IEEE conference on Design automation June 1988

A new simulated annealing schedule has been developed; its application to the standard cell placement and the traveling salesman problems results in a two to twenty-four times speedup over annealing schedules currently available in the literature. Since it uses only statistical quantities, the annealing schedule is applicable to general combinatorial optimization problems.

107 Delay macromodels for the timing analysis of GaAs DCFL 77%

A. I. Kayssi , K. A. Sakallah
Proceedings of the conference on European Design Automation November 1992

108 Near-optimal triangulation of a point set by simulated annealing 77%

Subhajit Sen , Si-Qing Zheng
Proceedings of the 1992 ACM/SIGAPP symposium on Applied computing: technological challenges of the 1990's March 1992

109 Timing driven placement using complete path delays 77%

Wilm E. Donath , Reini J. Norman , Bhuwan K. Agrawal , Stephen E. Bello , Sang Yong Han , Jerome M. Kurtzberg , Paul Lowy , Roger I. McMillan
Conference proceedings on 27th ACM/IEEE design automation conference January 1991

The Timing Drive Placement (TDP) system balances wirability and timing constraints so that the final released design meets timing criteria. This is achieved by dynamically evaluating the timing of critical paths during placement. TDP is significant because convergence to a timed wirable solution early in the physical design cycle is achieved, or else it becomes apparent that logic changes are required.

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Dynamic Thermal Management for High-Performance Microprocessors - Brooks, Martonosi (2001) (Correct) (12 citations)
Dynamic Thermal Management for High-Performance **Microprocessors** David Brooks Department of Electrical thermal packaging which can adequately **cool** the **processor**. It is estimated that after exceeding 35-40W, at run-time, to control a chip's operating **temperature**. Traditionally, the packaging and **fans** for a
www.ee.princeton.edu/~dbrooks/hpca2001.pdf

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Adaptive Thermal Management for High-Performance Microprocessors - Brooks, Martonosi (2000) (Correct) (5 citations)
Thermal Management for High-Performance **Microprocessors** David Brooks and Margaret Martonosi Dept. thermal packaging which can adequately **cool** the **processor**. It is estimated that after exceeding 35-40W, thresholds and generates an interrupt if the **temperature** crosses the threshold. In the PowerPC
www.ee.princeton.edu/~dbrooks/complex2000.ps

Dynamically Managing Processor Temperature and Power - Rohou, Smith (1999) (Correct) (7 citations)
more important issue in the design of future **microprocessors**. Maintaining the **temperature** of a **processor**
Dynamically Managing **Processor Temperature** and Power Erven Rohou and Michael
Dynamically Managing **Processor Temperature** and Power Erven Rohou and Michael D. Smith
www.eecs.harvard.edu/~erven/fdo.ps.gz

On the Limits and Applications of MEMS Sensor Networks - Pister (2001) (Correct) (1 citation)
power consumption in a power-optimized **microprocessor** vi is roughly 1nJ/instruction 2 This (ASICs) typically outperform general purpose **processors** by a factor of 100 to 1000 in the area of sensors)to work in buildings (that have **temperature** and motion sensors)which are all part of the
www-bsac.EECS.Berkeley.EDU/~tparsons/PisterPublications/2001/DSSG_Pister.pdf

Declustering Spatial Databases on a Multi-Computer Architecture - Nikos Koudas (1996) (Correct) (8 citations)
spatial access methods on multidisk or multi-**processor** machines. The majority of them examine the eg.x, y, z, time, pressure, wind velocity, **temperature**)or (gender, age, cholesterollevel, algorithm to achieve dynamic re-declustering, to '**cool**-off' hot spots is presented in [WZS91]However,
olympos.cs.umd.edu/pub/TechReports/edbt96.ps

Reducing Power in High-performance Microprocessors - Tiwari, Singh, Rajgopal.. (Correct) (21 citations)
Reducing Power in High-performance **Microprocessors** Vivek Tiwari, Deo Singh, Suresh Rajgopal, of the main curve indicate newer versions of each **processor** family. These are implemented in newer the devices below the specified operating **temperature** limits. Maintaining the integrity of packaging
herkules.informatik.tu-chemnitz.de/proceedings/dac-98/sun_sgi/../pdffiles/44_2.pdf

Feedback, Correlation, and Delay Concerns in the Power.. - Farid Najm (1995) (Correct) (7 citations)
will eventually be used. Specifically, for a **microprocessor** or a DSP chip, the data inputs can not be resulting high power dissipation elevates chip **temperature** and can cause performance degradation and and to their relative magnitudes over reconvergent **fan**out paths? This delay concern is dealt with in one
power.csl.uiuc.edu/~najm/papers/dac95-tutorial.ps

Power Estimation Techniques for Integrated Circuits - Najm (1995) (Correct) (5 citations)
a major concern in VLSI design [1, 2]Modern **microprocessors** are indeed hot, with typical power

and reduces chip lifetime. To control their **temperature** levels, high power chips require specialized signals may be correlated due to reconvergent **fanout** (a gate **fans** out into two signals that power.csl.uiuc.edu/~najm/papers/iccad95-tutorial.ps

An Energy-Complexity Model for VLSI Computations - Tierno (1995) (Correct) (2 citations)
a relatively efficient process. DEC's alpha **microprocessor**, for example, dissipates 36 W and can be :127 8 Example: **Processor** Design 128 8.1 Specification : : 121 7.2 **Temperature** Feed-Back : ftp.cs.caltech.edu/tr/cs-tr-95-02.ps.Z

Design Technologies for Low Power VLSI - Pedram (1997) (Correct) (1 citation)
Contemporary performance optimized **microprocessors** dissipate as much as 15-30 W at 100-200 MHz set-top computers and multimedia digital signal **processors**, the overall goal of power minimization is to High power systems often run hot, and high **temperature** tends to exacerbate several silicon failure vada.skku.ac.kr/Research/project/lp-pedram.pdf

Global Optimization Of Nonconvex Nonlinear Programs Using.. - Epperly (1995) (Correct) (1 citation)
Parallelism is achieved by applying a separate **processor** to the bounding of each region. Each **processor** reaction equilibrium problems at constant **temperature** can be solved by minimizing the Gibbs free osnome.che.wisc.edu/~epperly/thesis.ps.gz

Uniprocessor Performance Enhancement Through Adaptive Clock.. - Uht (2003) (Correct)
for a description of the first asynchronous **microprocessor** and [3] for a brief tutorial on modern in some laptop computers, the **temperature** of the **processor** is measured and fed back to control (throttle) adapt to their current surroundings (varying **temperature** conditions, etc.so as to increase or www.ssgrr.it/en/ssgrr2003w/papers/120.pdf

A Distributed Monitoring Mechanism for Wireless Sensor Networks - Hsin (Correct)
of the sensor or configured into the **microprocessor** software during the initial set up of the fault could include for example when the **temperature** or the volume of a certain chemical in the air Mechanism for Wireless Sensor Networks Chih-**fan** Hsin Advisor: Mingyan Liu EECS Department, www.eecs.umich.edu/~chsin/research/qual.pdf

Unknown - (Correct)
power consumption in a power-optimized **microprocessor** [6] is roughly 1 nanojoule (nJ) per (ASICs) typically outperform general-purpose **processors** by a factor of 100 to 1,000 in the area of sensors) to work in buildings (that have **temperature** and motion sensors)which are all part of the dssg.ida.org/pdf/paper2_1022.pdf

Tutorial and Survey Paper Power Minimization in IC.. - Massoud Pedram.. (Correct)
Contemporary performance optimized **microprocessors** dissipate as much as 15-30 W at 100-200 of the various components of a typical **processor** architecture is expressed as a function of a systems often run hot at the same time, high **temperature** tends to exacerbate several silicon failure www.inf.pucrs.br/~moraes/cp_papers/p3-pedram.pdf

SIMULATIONS OF GRAVITY WAVE INDUCED TURBULENCE USING 512.. - Iowa State University (Correct)
supercomputers, have been performed on the 512 **processor** Cray T3E machine at the National Energy velocity components (u v w)the potential **temperature**, water substance mixing ratios (vapor, cloud www.gfdl.gov/~ck/workshop/proceedings/prusa.ps

Lobster Robots - Ayers, Witting, Olcott, McGruer.. (Correct)
walking as a finite state machine on a sequential **processor** (Ayers and Crisman, 1992)We maintain several state (austenite) when annealed at high **temperatures**. When **cool**ed below the transition **temperature** when annealed at high **temperatures**. When **cool**ed below the transition **temperature** a nitinol wire www.dac.neu.edu/msc/lobsterrobots.pdf

An Energy-Efficient Leakage-Tolerant Dynamic Circuit.. - Wang, Krishnamurthy.. (Correct)
at Urbana-Champaign, Urbana, IL 61801. **Microprocessor** Research Laboratories, Intel Corporation, the worst-case leakage current (measured at room **temperature**) of low-V t and high- V t transistors are 25X

technique is proposed. Simulation results of wide **fan**-in gates designed in the Predictive Berkeley
www.icims.csl.uiuc.edu/~shanbhag/vips/publications/lei_asic00.pdf

Recognizing Local Weather Patterns with Traditional and Neural .. - Driesse, al. (Correct)
a data collection system implemented on a PDP-11 **processor** which monitored a weather station and a variety

speed, wind direction, sun strength, living room **temperature**, north bedroom **temperature**, south bedroom
8 o'clock in the evening, i.e. when the outdoor air **cools** and inside humidity increases due to cooking
www.cas.mcmaster.ca/cas/research/dcssreports/DCSSTR9602.pdf

Are you interested in Computers and Electronics? - David Abramson Gordon (Correct)
platform, we based it on an existing embedded **microprocessor**, keeping the chip count low and increasing
instruction set computer, a PIC18F8X [10]This **processor** is much less powerful than the type found in a
system, it is possible to monitor light level, **temperature**, window and door status and who is currently
www.csse.monash.edu.au/~davida/papers/smarthouse.pdf

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Overview NASA Scatterometers Projects - Graf, al. (Correct)
the return ethos using an on-board digital **processor**. Key NSCAT system are given in Table 1. Fig.
to maintain the instrument in the operational **temperature** via a passive control scheme (louver)will be
consists of six identical, dual-polarization **fan** beam antennas. Each antenna is made up of two
jpltrs.jpl.nasa.gov/1995/95-0657.pdf

Rapid Prototyping for Fuzzy Systems - Chantrapornchai, Tongsima, Sha (1996) (Correct)
[9, 16]Some researchers focus on designing **processor** architectures for fuzzy logic controllers [2,
1(a) shows an example of rule base for a simple **temperature** control system. The corresponding FRA is
shown
has 3 internal IF **temperature** is hot THEN set the **fan** speed to fast IF **temperature** is cold THEN set
irish.hpcc.nectec.or.th/~stongsim/research/conf/glsvlsi96.ps

A High Performance 180 nm Generation Logic Technology - Yang Ahmed Arcot (Correct)
Transistor performance still dominates overall **microprocessor** speed and aggressive gate oxide and gate
= 1) operating at 1.3 V and 1.5 V and at room **temperature**. The delay per stage at minimum gate lengths
delay vs. gate length for unloaded ring oscillators (**fan** out =1) operating at 1.3 V and 1.5 V and at room
www.wam.umd.edu/~davewang/Intel180nm.pdf

In-Cylinder Measurement for Engine Cold-Start Control - Tunestl, Wilcutts, Lee.. (Correct)
and the advent of cheap, powerful digital signal **processors**, the hurdles to the use of cylinder pressure
ineffective until they reach "light-off" **temperature** of 250300 C. During starting and idling, the
starting and idling, the low flow of relatively **cool** exhaust gases takes several minutes to accomplish
vehicle.me.berkeley.edu/~pert/ccadoc.pdf

A 20 Ampere Shunt Regulator For Controlling Individual.. - Martin Dobeck Jones (1995) (Correct)
complete electrical isolation, an onboard **microprocessor** provides remote communications via an
lead clears and the blown fuse is reported to the **processor**. Load current is re-distributed equally amongst
from a manganin shunt maintained at a constant **temperature** for stability. The module is designed for
www.aps.anl.gov/conferences/mirrored/www.cern.ch/accelconf/p95/ARTICLES/RPP/RPP06.PDF

Study Of Unk Quench Protection System On The String.. - Andriischin.. (Correct)
modules common for all cell: timer, 16-bit **microprocessor**, RAM, interface and input/output module. AMP
at the exterior of the cryostats at the ambient **temperature** and energy removal from the remaining part of
a steel tube 200mm in diameter for imitation the **cool**ing conditions at the UNK tunnel, where they have
www.aps.anl.gov/conferences/mirrored/www.cern.ch/accelconf/p95/ARTICLES/FAQ/FAQ06.PDF

RSFQ Subsystem for Petaflops-Scale Computing: "COOL-0" - Paul Bunyk Mikhail (Correct)
performance. The RSFQ subsystem consists of **processors** (SPELLs)cryoelectronic memory, and switching
elements (SPELLs) operating at liquid helium **temperature**. A powerful method of hiding memory access
RSFQ Subsystem for Petaflops-Scale Computing: **COOL**-0" Paul Bunyk Mikhail Dorojevets
gamayun.physics.sunysb.edu/pub/rsfq/isec99-1.ps

Parallelizing Appbt for a Shared-Memory Multiprocessor - Ce Ss Or (Correct)
protocols for machines ranging from 1 to 128 **processors**. We found that our parallelization methodology
its engine. The time-dependent solution for the **temperature**, pressure, and velocity is desired at various
ftp.cs.wisc.edu/pub/tech-reports/ncstrl.uwmadison/CS-TR-95-1286/CS-TR-95-1286.ps.Z

Satisfiability Test with Synchronous Simulated Annealing on.. - Andrew Sohn Cis (Correct)
while giving almost a 70-fold speedup on 500 **processors**. 1 INTRODUCTION The Satisfiability (SAT)
analogy the way metals **cool** and anneal as their **temperatures** decrease. A typical implementation of SA

method is based on the analogy the way metals **cool** and anneal as their **temperatures** decrease. A
science.nas.nasa.gov/~rbiswas/HTML/../PAPERS/ics96.ps

cessful. Permanent installation was not reached because of.. - Adaptive Control In (Correct)
practice [210, 133, 211]A prototype of a **microprocessor** probe as a control expert advisor has been
square-root controllers. A triangular array of **processors** solves one step of dynamic programming in six
(about 1m)ffl Installation of adaptive **temperature** control within a rotary kiln used in
www.utia.cas.cz/user_data/scientific/AS_dept/info97.ps

Superconductor Multithreaded Subsystem for Petaflops Scale.. - Mikhail Dorojevets (Correct)
multiple levels of memory and three types of **processors**: SRAM and DRAM **Processor**-In-Memory (PIM)
(PIM) elements operating at room **temperature**, and ultrafast Superconductor Processing
RSFQ technology. We consider a proposed parallel **COOL** architecture and its possible implementation in a
gamayun.physics.sunysb.edu/pub/rsfq/isscc98.ps

Mechanical Design Of The Cdf Svx Ii Silicon Vertex Detector - John Skarha (Correct)
top and b physics analyses. A Level 2 trigger **processor**, the Silicon Vertex Tracker (SVT)7 will
order to minimize stresses in the silicon during **temperature** changes. The ladder support structure should
The kapton/beryllium combination should have good **cool**ing performance and lower mass than standard thick
www-cdf.fnal.gov/physics/conf94/cdf2759_svxii_mech_dpf.ps

System and Circuit Aspects of Nanoelectronics - Goser, Pacha (1998) (Correct)
systolic arrays, a propagate instruction array **processor**, and fault tolerant logic. Furthermore,
devices because they already operate at room-**temperature**. Moreover, from the viewpoint of circuit
have sufficient driving capability and at least a **fan**-out of 2. ffl A small leakage current in the
www-be.e-technik.uni-dortmund.de/~pacha/lit/goseress.ps.Z

Implementing Fuzzy Control Systems Using VHDL and Statecharts - Salapura, Hamann (Correct)
rather then to extend some general purpose **processor** with fuzzy instructions. Our decision is
input variables delivered by sensors: the room **temperature** and, assuming there is no stable gas quality,
divided into three overlapping fuzzy sets called "**cool**"tepid"and "warm"A similar classification
www.vlsivie.tuwien.ac.at/vanja/papers/edacV.ps

Applications of Single-Electron Transistors - Costa, Goossens, Verhoeven.. (Correct)
by the semiconductor industry for memory and **processor** fabrication should attain the limits imposed by
singleelectron transistors operating at room **temperature** [8]indicates that the transition from
charges and their fluctuations [19]20]limited **fan** in (10) and **fan** out (3) in present day
www.stw.nl/prorisc/workshop/proc/psz/camargo.ps.gz

N-ary Speculative Computation of Simulated Annealing on the.. - Andrew Sohn (Correct)
execute n different iterations in parallel on n **processors**, called Generalized Speculative Computation
www.cis.njit.edu/sohn/papers/tpds95.ps.gz

t/hadron Processor System for the ATLAS First-Level Trigger - Perera Edwards (Correct)
The e/g and t/hadron **Processor** System for the ATLAS First-Level Trigger V.
may be extended to 1800 Mbaud over a reduced **temperature** range (0 0 C to 65 0 C)The requirement
in sixteen different windows, implying a massive **fan**-out of signals. To keep the **fan**-out and the pin
sunset.roma1.infn.it/LEB98/proceedings/perera.ps

Simulated Annealing for N-body Systems - Voogd Sloot (1994) (Correct)
chain is assigned to each of the available **processors**. All chains have equal length. The chains are
annealing a material is heated to a high **temperature**, and then allowed to **cool** slowly. At high
heated to a high **temperature**, and then allowed to **cool** slowly. At high **temperature** the system can explore
www.wins.uva.nl/research/pscs/projects/../papers/archive/Voogd94_1.ps.gz

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Parallel Satisfiability Test with Synchronous Simulated Annealing.. - Sohn (1996) (Correct)
while giving almost a 70-fold speedup on 500 **processors**. 2 1 Introduction The Satisfiability (SAT) analogy the way metals **cool** and anneal as their **temperatures** decrease. A typical implementation of
www.cis.njit.edu/sohn/papers/jpdc-sat.ps.gz

Parallel Rejectionless Annealing for Discrete Combinatorial.. - Kwiatkowski, Roe (Correct)
then communicates at step 6, synchronising the **processors** with a global update of the state s. Figure 3 in metals, where the metal is heated to a high **temperature**, below it's melting point and maintained at at that **temperature**. The metal is then allowed to **cool**, at a defined **cool**ing rate to produce a metal with
www.fit.qut.edu.au/~proe/papers/part96nik.ps.gz

Basic Science and Challenges in Process Simulation - Dabrowski, Mussig, Duane.. (1999) (Correct)
the products shipped in 1997 by a prospering **microprocessor** company may have been made with "old" 0.5 and
epi or implanted layers) is very promising. Most **processor** structures use it (Intel: 100%Quantitative [10]High-quality gate oxides are grown by high-**temperature** dry oxidation after striping the remaining pad
www.ihp-ffo.de/chipps/97/Ddoc/dpg.ps

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1 **A dual differential charge-coupled analog delay device**
Sealer, D.A.; Tompsett, M.F.;
Solid-State Circuits, IEEE Journal of , Volume: 11 Issue: 1 , Feb 1976
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[Abstract] [PDF Full-Text (672 KB)] **IEEE JNL**

2 **A new single-chip C/SUP 2/MOS A/D converter for microprocessor systems-Penta-Phase Integrating C/SUP 2/MOS A/D converter**
Suzuki, Y.; Masuda, E.; Satoh, C.; Iida, T.;
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Laber, C.A.; Gray, P.R.;
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[Abstract] [PDF Full-Text (744 KB)] **IEEE JNL**

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[Abstract] [PDF Full-Text (624 KB)] **IEEE JNL**

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9 **GaAs MESFET digital integrated circuits fabricated with low temperature buffer technology**
Delaney, M.J.; Chou, C.S.; Larson, L.E.; Jensen, J.F.; Deakin, D.S.; Brown, A.S.; Hooper, W.W.; Thompson, M.A.; McCray, L.G.; Rosenbaum, S.E.;
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Klinkhachorn, P.; Huner, B.; Overton, E.B.; Dharmasena, H.P.; Gustowski, D.A.;
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[Abstract] [PDF Full-Text (368 KB)] **IEEE CNF**

11 **Micropower analog structures for a CMOS heart rate indicator**
Ruha, A.; Kostamovaara, J.; Saynajakangas, S.;
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[Abstract] [PDF Full-Text (460 KB)] **IEEE JNL**

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[Abstract] [PDF Full-Text (200 KB)] **IEEE JNL**

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Takabatake, M.; Ohwada, J.; Ono, Y.A.; Ono, K.; Mimura, A.; Konishi, N.;

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Gautier, J.; Guegan, G.; Guerin, M.; Lerme, M.;
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De Cock, B.A.; Maurissens, D.; Cornelis, J.;
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26 **Continuously variable gigahertz phase-shifter IC covering more than one frequency decade**
Schmidt, L.; Rein, H.-M.;
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